

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1-15, 17-19 and 24-25 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 1-2, 6-8 and 24-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Herring (US 6,606,326) in view of Calamvokis et al. (US 5,592,476).

For claim 1, Herring discloses packet switch employing dynamic transfer of data packet from central shared queue path to cross-point switching matrix path, comprising:

a first port (figure 3, reference 310) to receive a network packet (col. 12, lines 11-

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12);

a second port (figure 3, reference 380) in communication with the first port (figure 3, reference 310), the second port to transmit the network packet after processing (col. 12, line 24);

circuitry (figure 1, reference 15) to associate first control information with a first portion of the network packet and to associate second control information with a second portion of the network packet (col. 9, lines 30-39); and

circuitry (figure 1, reference 15) to process the first portion of the network packet and to process the second portion of the network packet at least partially in parallel with processing the first portion of the network packet (col. 9, lines 30-39).

However, Herring does not expressly disclose circuitry to enqueue the first portion and the second portion for transmission to a second port in the same order in which the first portion and the second portion were received at the first port.

In an analogous art, Calamvokis et al. disclose circuitry to enqueue the first portion and the second portion for transmission to a second port (col. 7, line 57 to col. 8, line 1) in the same order in which the first portion and the second portion were received at the first port (col. 7, lines 48-56).

One skilled in the art would have recognized the circuitry to enqueue the first portion and the second portion for transmission to a second port in the same order in which the first portion and the second portion were received at the first port, and would have applied Calamvokis et al.'s controller 33 in Herring's processing element 15.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the

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invention, to use Calamvokis et al.'s asynchronous transfer mode switch with multicasting ability in Herring's packet switch employing dynamic transfer of data packet from central shared queue path to cross-point switching matrix path with the motivation being to provide the output port serviced in a fixed order as the same strict order serviced in the input port for the headers and cell body addresses of incoming cells (col. 7, lines 48-49, and col. 7, lines 65-66).

For claim 2, Herring discloses wherein the circuitry comprises:

one or more peripheral buses (figure 3, reference 315 and 370, col. 12, lines 35-42);

a memory system (figure 4, references 410, 420, 430 and 440, col. 15, lines 36-45);

a processor (figure 3, reference 340) coupled to the one or more peripheral buses and the memory system, the processor adapted to forward data from the first port to the second port (col. 14, lines 13-19); and

a bus interface to receive the first portion of the network packet and the second portion of the network packet from the first port and enqueueing the first portion and the second portion in the order in which they were received from the first port for transmission to the second port, the first and second portions being processed at least partially in parallel (col. 16, lines 45-50).

For claim 6, Herring discloses wherein the one or more peripheral buses comprise at least one input-output bus, wherein the processor is adapted to interface over the input-output bus with at least one of a media access controller device and a

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high-speed device, the high-speed device comprising at least one of a gigabit Ethernet MAC and a dual gigabit MAC with two ports (figure 3, reference 315 and 370, col. 12, lines 35-42).

For claim 7, Herring discloses wherein the memory system further comprises at least one of a random access memory, a synchronous dynamic random access memory, a synchronous dynamic random access memory controller, a static random access memory controller, and a nonvolatile memory (figure 4, references 410, 420, 430 and 440, col. 15, lines 36-45).

For claim 8, Herring discloses wherein the memory system further comprises a memory bus, wherein the memory bus is adapted to couple one or more bus interfaces to one or more memory controllers (figure 4, references 410, 420, 430 and 440, col. 15, lines 36-45).

For claim 24, Herring discloses packet switch employing dynamic transfer of data packet from central shared queue path to cross-point switching matrix path, comprising:

receiving means to receive a network packet at a first port (figure 3, reference 310) (col. 12, lines 11-12);

transmitting means for transmitting the network packet after processing, the receiving means in communication with the transmitting means (col. 12, line 24);

means for associating a first control information with a first portion of the network packet (col. 9, lines 30-39);

means for associating second control information with a second portion of the network packet (col. 9, lines 30-39); and

means for processing the first portion of the network packet and the second portion of the network packet at least partially in parallel (col. 9, lines 30-39).

However, Herring does not expressly disclose means for circuitry to enqueue the first portion and the second portion for transmission to a second port in the same order in which the first portion and the second portion were received at the first port. In an analogous art, Calamvokis et al. disclose means for circuitry to enqueue the first portion and the second portion for transmission to a second port (col. 7, line 57 to col. 8, line 1) in the same order in which the first portion and the second portion were received at the first port (col. 7, lines 48-56).

One skilled in the art would have recognized the means for circuitry to enqueue the first portion and the second portion for transmission to a second port in the same order in which the first portion and the second portion were received at the first port, and would have applied Calamvokis et al.'s controller 33 in Herring's processing element 15. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, to use Calamvokis et al.'s asynchronous transfer mode switch with multicasting ability in Herring's packet switch employing dynamic transfer of data packet from central shared queue path to cross-point switching matrix path with the motivation being to provide the output port serviced in a fixed order as the same strict order serviced in the input port for the headers and cell body addresses of incoming cells (col. 7, lines 48-49, and col. 7, lines 65-66).

For claim 25, Herring discloses wherein the means for processing the first portion of the network packet and the second portion of the network packet at least partially in parallel is implemented at least partially in software (col. 9, lines 30-34).

5. Claims 3-5 and 9-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Herring (US 6,606,326) in view of Calamvokis et al. (US 5,592,476) further in view of Rosborough et al. (US 6,493,754).

For claims 3-5 and 9, Herring disclose wherein the processor comprises one or more microengines (figure 1, reference 15, col. 9, lines 31-34) to execute program threads, the threads include receive schedule program threads to assign the first portion of the network packet from the first port to a first receive processing program thread and the second portion of the network packet to a second receive processing program thread, wherein the bus interface is responsive to the one or more microengines, and wherein the first and second receive processing program threads are adapted for processing and enqueueing (figure 3, reference 350)(col. 12, lines 35-38).

Herring disclose wherein the processor comprises one or more microengines (figure 1, reference 15) to execute program, wherein the one or more microengines are configured to operate with shared resources, and wherein the shared resources comprise the memory system (figure 4, references 350 and 410-440) and the one or more peripheral buses (figure 3, reference 315 and 370)(col. 9, lines 30-34 as set forth in claim 9).

However, Herring in view of Calamvokis et al. does not expressly disclose program threads. In an analogous art, Rosborough et al. disclose program threads (col. 6, line 39).

Rosborough et al. disclose wherein the bus interface uses sequence numbers to enqueue the first portion and the second portion, wherein the bus interface is to associate one or more first portion sequence numbers with the first portion and one or more second portion sequence numbers with the second portion as the first and second portions are received from the first port (col. 9, lines 35-42 as set forth in claim 4); wherein the bus interface is further to maintain a second set of sequence numbers for use by the first and second receive processing program threads in determining the order in which the first and second portions are to be enqueued (col. 9, lines 35-42 as set forth in claim 5);

One skilled in the art would have recognized the program threads, and would have applied Rosborough et al.'s threads in Herring's processing element 15. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, to use Rosborough et al.'s method and apparatus for analyzing communications on different threads in Herring's packet switch employing dynamic transfer of data packet from central shared queue path to cross-point switching matrix path with the motivation being identified such that it can have only one service request on it at a given point in time (col. 6, lines 44-48).

For claim 10, Herring disclose wherein the bus interface comprises an input-output bus interface (figure 3, reference 315 and 370, col. 12, lines 35-42).

For claim 11, Herring disclose wherein the bus interface is coupled to an input-output bus, wherein the input-output bus is coupled to a dual gigabit MAC (figure 3, reference 315 and 370, col. 12, lines 35-42).

For claim 12, Herring disclose wherein at least one of the microengines comprises:

a control store for storing a microprogram; and a set of control logic, wherein the set of control logic comprises an instruction decoder and one or more program counter units (col. 14, lines 13-18).

For claim 13, Herring disclose wherein at least one of the microengines further comprises a set of context event switching logic to receive messages from the shared resources (col. 14, lines 13-18).

6. Claims 14-15 and 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Herring (US 6,606,326) in view of Boucher et al. (US 6,226,680) further in view of Calamvokis et al. (US 5,592,476).

For claim 14, Herring discloses packet switch employing dynamic transfer of data packet from central shared queue path to cross-point switching matrix path, comprising:

controller (figure 3, reference 340) comprising one or more ports (figure 3, references 310 and 380, col. 11, lines 62-65).

However, Herring does not expressly disclose:

a media access controller capable of providing one or more status flags;

a bus interface unit comprising one or more registers, wherein the one or more registers comprise control registers and status registers;

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a bus connected between the media access controller and the bus interface unit;
a sequencer to poll the one or more status flags and place the one or more status flags to the one or more registers over the bus, wherein the communication system is capable of processing one or more packets of data, and wherein the communication system is capable of maintaining an intra-packet order and an inter-packet order for the one or more ports; and

wherein the communication system is capable of enqueueing a first portion of a network packet and a second portion of a network packet for transmission to a second port in the same order in which the first portion and the second portion were received at a first port.

In an analogous art, Boucher et al. disclose:

a media access controller (figure 13, references 210) capable of providing one or more status flags (col. 18, lines 27-29);

a bus interface unit (figure 13, reference 468) comprising one or more registers (figure 14, references 490, 496 and 501), wherein the one or more registers comprise control registers and status registers (col. 16, lines 64-65);

a bus connected between the media access controller (figure 13, references 210) and the bus interface unit (figure 13, reference 468); and

a sequencer (figure 7, reference 176) to poll the one or more status flags and place the one or more status flags to the one or more registers over the bus, wherein the communication system is capable of processing one or more packets of data, and

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wherein the communication system is capable of maintaining an intra-packet order and an inter-packet order for the one or more ports (col. 9, line 66 to col. 10, line 4).

Boucher et al. disclose wherein the media access controller further comprises one or more transmit registers and one or more receive registers, and wherein the one or more ports comprise at least two gigabit Ethernet ports (col. 16, lines 64-65 as set forth in claim 15); wherein the one or more status flags comprise one or more transmit status flags and one or more receive status flags, and wherein the one or more flags indicate whether an amount of data in associated transmit registers and associated received registers have reached a threshold level (col. 18, lines 27-29 as set forth in claim 17); wherein a receive scheduler thread uses the one or more registers in the bus interface unit to determine how to issue a receive request (col. 17, lines 7-12 as set forth in claim 18); and wherein the communication system uses a set of sequence numbers for each port, wherein the sequence numbers comprise a network packet sequence number, a MAC packet sequence number, and an enqueue sequence number (col. 10, lines 27-35 as set forth in claim 19).

One skilled in the art would have recognized the media access controller, and would have applied Boucher et al.'s media access controller 172 in Herring's processing system 5. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, to use Boucher et al.'s intelligent network interface system method for protocol processing in Herring's packet switch employing dynamic transfer of data packet from central shared queue path to cross-point switching matrix path with the motivation being received message packet (col. 9, line 55).

However, Herring in view of Boucher et al. does not expressly disclose wherein the communication system is capable of enqueueing a first portion of a network packet and a second portion of a network packet for transmission to a second port in the same order in which the first portion and the second portion were received at a first port.

In an analogous art, Calamvokis et al. disclose wherein the communication system is capable of enqueueing a first portion of a network packet and a second portion of a network packet for transmission to a second port (col. 7, line 57 to col. 8, line 1) in the same order in which the first portion and the second portion were received at a first port (col. 7, lines 48-56).

One skilled in the art would have recognized the wherein the communication system is capable of enqueueing a first portion of a network packet and a second portion of a network packet for transmission to a second port in the same order in which the first portion and the second portion were received at a first port, and would have applied Calamvokis et al.'s controller 33 in Herring's processing element 15. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, to use Calamvokis et al.'s asynchronous transfer mode switch with multicasting ability in Herring's packet switch employing dynamic transfer of data packet from central shared queue path to cross-point switching matrix path with the motivation being to provide the output port serviced in a fixed order as the same strict order serviced in the input port for the headers and cell body addresses of incoming cells (col. 7, lines 48-49, and col. 7, lines 65-66).

Conclusion

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7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to TOAN D. NGUYEN whose telephone number is (571)272-3153. The examiner can normally be reached on M-F (7:00AM-4:30PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, William Trost can be reached on 571-272-7872. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/T. D. N./
Examiner, Art Unit 2416

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Supervisory Patent Examiner, Art Unit 2416